



## Spring 2010 CIS Colloquium Series

### Exploring Network-on-Chip (NoC) Architecture Design Space

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*3-4pm, Monday, May17*

*4<sup>th</sup> Floor Conference Room (Wachman Hall, CC 447)*

**Abstract:** Integration of multiple cores on the same chip has signaled the beginning of communication-centric, rather than computation-centric systems. Further, technology trends have accentuated the importance of interconnect-conscious design as global wire delays do not scale down as fast as gate delays in new technologies. Consequently, on-chip interconnects, also known as Network-on-Chip (NoC) architectures, are predicted to become a major bottleneck in designing embedded System-on-Chip (SoC) architectures and high-performance multi-core architectures alike. However, unlike the traditional multiprocessor interconnects, design of scalable and high performance on-chip interconnects poses a whole set of new challenges in terms of on-chip area budget, energy/thermal efficiency, and reliability constraints. Consequently, to combat the growing concerns of interconnect designs, new architectural and technological solutions are being actively pursued. In this talk, we will discuss the NoC design challenges and summarize plausible solutions encompassing performance, scalability, power, thermal and reliability issues. The talk will summarize two of our ongoing projects: application-aware NoC design and tunable frequency routers for NoCs.

*Refreshments will be served!*